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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/247,413 02/10/99 LO

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020808
BROWN PINNISI & MICHAELS
400 M & T BANK BUILDING
118 NORTH TIoga ST
ITHACA NY 14850

IM62/0107

EXAMINER

ANDERSON, M

ART UNIT

PAPER NUMBER

1785

DATE MAILED:

5
01/07/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/247,413

Applicant(s)
Lo et al.

Examiner
Matt Anderson

Group Art Unit
1765



☒ Responsive to communication(s) filed on 2/10/99

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-17 is/are pending in the application

Of the above, claim(s) 14-17 is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-13 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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DETAILED ACTION

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-13, drawn to method , classified in class 117 , subclass 1.
- II. Claims 14-17, drawn to product, classified in class 257 , subclass 615.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions and are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process as claimed can be used to make another and materially different product of a GaN laser diode on a sapphire substrate.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

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4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Michael Brown on 12/12/99 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-13. Affirmation of this election must be made by applicant in replying to this Office action. Claims 14-17 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

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Claim Rejections - 35 U.S.C. § 112

8. Claims 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. Claim 12 has no physical steps. Claim 13 is rejected as being dependent to Claim 12. Claim 12 has been examined as if it were incorporated with claim 13.

Claim Rejections - 35 U.S.C. § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1,7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimbo et al. (US 4,738,935).

Shimbo et al. discloses the bonding of GaP and InP in Figs. 2A and 2B. The mental steps described in Claim 1 would be performed inherently during the well known procedure of 'lattice engineering' of III-V semiconductor compounds.

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Claim Rejections - 35 U.S.C. § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 2-4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimbo et al. as applied to claims 1, 7-8 above, and further in view of Lee et al. (US 4,900,372).

Shimbo et al. discloses the bonding of InP and GaP substrates as described above.

Shimbo et al. does not describe the so formed device as a substrate for further fabrication.

Lee et al. discloses in the abstract a method of annealing deposited layers of III-V compound semiconductors when deposited on Si, Ge/Si, or other single crystal substrates. In Col. 3 lines 42+ is described the formation of a thermal strain layer (i.e. a buffer layer) and its anneal cycle. Lee et al. in Col. 4 lines 1-17 describe typical buffer layers as GaAs, InGaAs, and AlGaAs. The second buffer layer is described as also annealed. One of ordinary skill in the art would recognize the anneal steps as for the purpose of reducing the crystal imperfections in the buffer layers.

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It would have been obvious to combine the references of Shimbo et al. and Lee et al. because Shimbo et al. produces a construct which would be useful as a substrate and Lee et al. discloses the formation of a buffer layer thereon and because such a combination would have been anticipated to produce an expected result.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to grow the buffer layer on either face of the substrate because Lee discloses the formation of a buffer layer on a single crystal substrate (of which, a InP/GaP bonded substrate is one) and because such a combination would have been anticipated to produce an expected result.

13. Claims 5-6, 9-11,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimbo et al. and Lee et al. as applied to claim s 1-4,7-8 above, and further in view of Lee et al. (US 4,900,372).

Shimbo et al. discloses the bonding of InP and GaP substrates as described above.

Shimbo et al. does not describe further device fabrication.

Lee et al. discloses a method of annealing deposited layers of III-V compound semiconductors when single crystal substrates as described above..

Lee does not disclose further device fabrication after the buffer layer.

Furuyama et al. discloses a semiconductor device as is seen in Fig. 5. InP has GaInAs deposited thereon. InP is seen to be deposited thereon with a further deposition of InP (an InP based semiconductor).

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It would have been obvious to one of the ordinary skill in the art at the time of the present invention to combine the references because all dealt with III-V semiconductors and because such a combination would have been anticipated to produce an expected result.

It would have been obvious to grow a first epilayer (InP) on a buffer layer (GaInAs intermediate buffer layer) and a second epilayer (InP) on the first epilayer because such a growth sequence was suggested in the art (Furuyama et al.) and because such a growth sequence would have been anticipated to produce an expected result.

It would have been obvious at the time of the present invention to one of ordinary skill in the art to for the buffer layer from AlGaAs, or InGaAs and the first and second epilayers from InP because such materials are suggested by the combined references and because such a use of these materials would have been anticipated to produce an expected result.

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14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Anderson whose telephone number is (703) 308-0086. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Benjamin Utech, can be reached at (703) 308-3836.

Any inquiry of a general nature can be directed to the group receptionist whose telephone number is (703) 308-0661.


BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

MAA

January 5, 2000